



IR-2550 DIV (2-3619)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of
Martin Standing et al.
Serial No.: 10/634,447
Filed: August 5, 2003

New York, New York
Date: January 11, 2005
Group Art Unit: 2811
Examiner: Unassigned

For: CHIP SCALE SURFACE MOUNTED DEVICE AND PROCESS OF MANUFACTURE

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SUBMISSION

Sir:

Submitted herewith is a copy of art together with a form listing the same for the convenience of the Examiner.

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents P.O. Box 1450, Alexandria, VA 22313-1450, on January 11, 2005

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Name of applicant, assignee or
Registered Representative

Signature

January 11, 2005

Date of Signature

Respectfully submitted,

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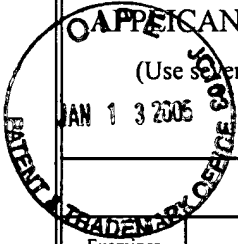
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Enclosures

APPLICANT'S ART CITATION (Use several sheets if necessary) 	Application 10/634,447	OFGS File No. IR-2550 DIV (2-3619)
	Applicant Martin Standing et al.	
	Filing Date August 5, 2003	Group Art Unit 2811

U.S. PATENT DOCUMENTS (not submitted for applications filed after 6/30/03)

Examiner Initial	Document Number	Date MM-YYYY	Name	Class	Sub-class	Filing Date If Appropriate
	US-6,744,124	06-2004	CHANG ET AL.			
	US-					
	US-					
	US-					
	US-					
	US-					
	US-					
	US-					
	US-					

FOREIGN PATENT DOCUMENTS

	Document Number	Date MM-YYYY	Country	Class	Sub-class	Translation	
						Yes	No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

		MOSFET BGA DESIGN GUIDE 2004-FAIRCHILD SEMICONDUCTOR, pages i-ii and pages 1-43

Examiner	Date Considered
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EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.